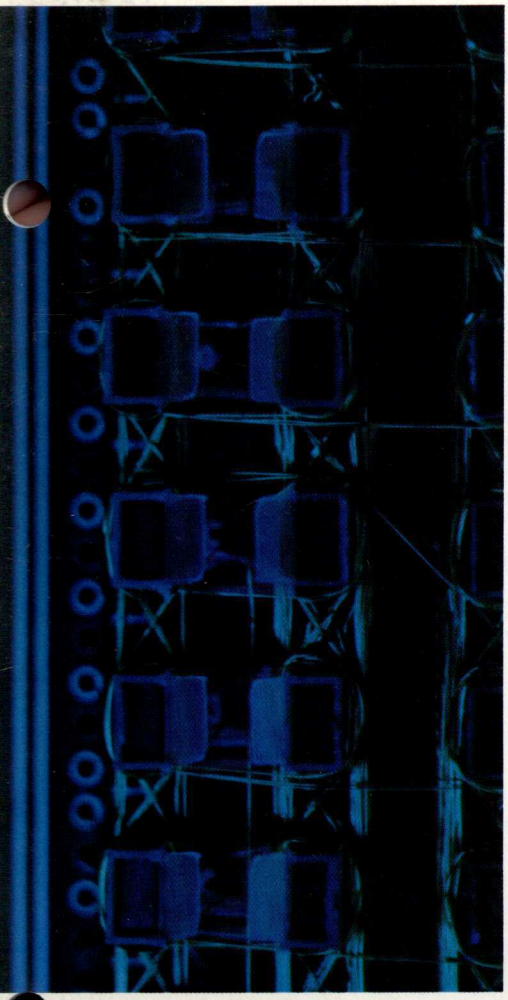


The Model 5

≈1970

INTERDATA®

Introduction

The INTERDATA Model 5 represents a logical extension of the most successful family of small 3rd generation computers ever conceived. As an outgrowth of the widely accepted INTERDATA Model 4, the new Model 5 was literally designed by you, the user. We have incorporated into the Model 5 all of the flexibility and features that programmers, systems engineers and management told us they wanted in a general purpose computer—and, at the right price. But the Model 5 is only part of the story.

Behind our new computer is a sound management team that had the courage to implement your ideas, to make a long range investment in computer development...an efficient manufacturing team and complete support facilities.

With hundreds of installed systems in the general purpose and communication field, INTERDATA is eminently qualified to serve you on an OEM or user basis.

Take the next few minutes and acquaint yourself with the new Model 5, and what it can mean to your business.

Introducing the Model 5

A Multi-Task Systems Computer The Model 5 is an important advance in the design of systems computers. Through strategic combinations of hardware, software and firmware, we have structured a multi-task approach to the solution of systems problems. This achievement is an outgrowth of the principles which INTERDATA first brought to our industry, namely **3rd generation architecture, Read Only Memory and firmware.**

True Foreground/Background Capability—The Model 5 offers, for the first time in a moderate price range, a computer with true multi-task capability. This is accomplished through a number of built-in features for interrupt and I/O handling, processing power, and a unique program protection mechanism for isolating foreground from background. Priviledged instructions and memory protect controls, which are integral parts of the Model 5 processor, provide a unique program protection mechanism. Thanks to these features the Model 5 can concurrently manage a multitude of process-oriented tasks such as real-time data collection, communications and control. Unused processor time can be safely made available for background processing without risking the integrity of foreground operations.

Large Computer Features—Memory protect and priviledged instructions make the Model 5 outstanding in its class. This means that application programs, compilations and data processing can be safely performed on-line. The Model 5's operations are enhanced by 16 levels of priority interrupt, and a firmware-driven I/O channel for concurrent I/O operations and processing. The Model 5's processing tasks benefit from 3rd generation architecture and an extensive instruction set, including floating-point operations, list processing and byte-handling instructions.

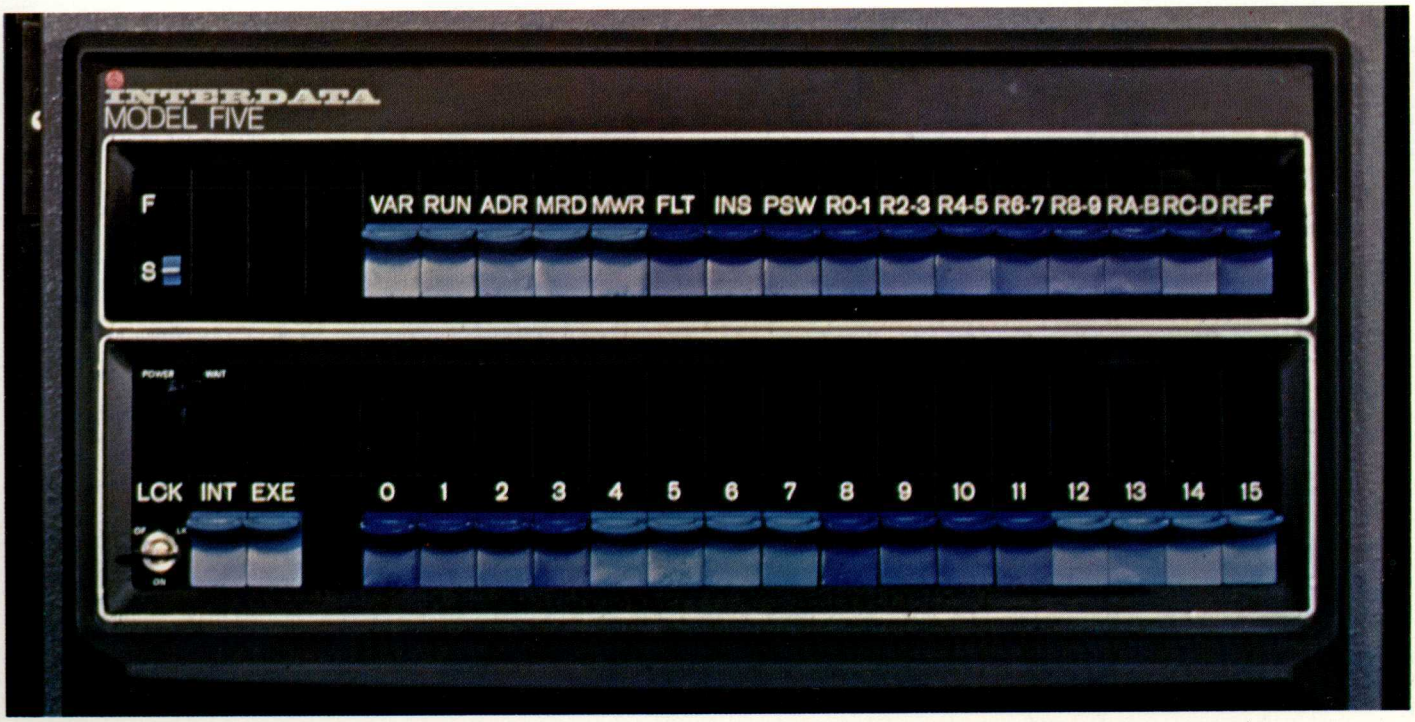
Besides its sophisticated instruction set, the Model 5 has many features you would normally find only in much larger computers: 16 general purpose registers for use as accumulators or index registers, direct core addressability to 64K bytes, immediate operands and a full complement of peripherals and interfaces.

Multiple Task Software—Software systems are designed to coordinate multi-task operations. Its Real-Time Operating System permits a variety of tasks to be run concurrently. This permits a number of real-time applications to be managed at the same time, while also permitting new programs to be compiled, assembled and debugged safely. Programs can be written in both Fortran and Assembly languages.

Cost/Performance Breakthroughs The capabilities and performance of the Model 5 can't be matched unless you are prepared to spend a lot more. Moreover, we have achieved two additional cost breakthroughs — a 64K byte mass core option that costs less than half of what you would expect to pay, and a digital multiplexor option that handles up to 2048 inputs and outputs — also at a fraction of the usual cost.

Instrumentation System Application For multi-instrument data acquisition requirements the Model 5's foreground system is well suited to handling burst transfers at peak rates. Its background system can be partitioned to perform data reduction and analysis in real time. At lower priority it can be safely used to assemble, compile and debug experimental programs.

Process Control Applications—For process control requirements, the Model 5 offers powerful advantages. Its foreground system is well suited to the real time scanning of hundreds of instrument readings, process alarms and pulse trains. In a protected background mode, process control programs can be compiled, assembled and tested without danger to the process. The Model 5's I/O Processor is particularly helpful in applications where a large amount of main processor time is needed for parallel computations.



Manufacturing Applications – The Model 5 with its digital multiplexor option is an ideal processor for the monitoring of hundreds of on-line data collection stations throughout a factory. At the same time the Model 5 has the real-time capacity for taking instrument readings from numerous quality control stations. In the background, the system can be safely used for inquiry processing, report generation and data communications.

Data Communication Systems – For high speed terminal handling, control and communications applications, the foreground/background system in the Model 5 has impressive capacity. While the foreground manages I/O transfers, multiplexing and data concentration — the background is well suited to message formatting, file management and local data processing.

Model 5 Architecture

The major sub-systems which comprise the Model 5 are task-oriented elements whose arrangement is depicted in the block diagram. The structure of the system is made flexible and expandable by unique Memory Bus and Multiplexor I/O Bus systems. This means that a variety of combinations are possible and can be rearranged and expanded in the field. Standard configurations with associated software are identified in the chart on the opposite page.

The Model 5 Processor Element This element incorporates a 400 nanosecond microcoded processor whose pre-programmed Read Only Memory controls arithmetic and logical functions as well as internal and external mechanisms of data transfer. These pre-programmed micro-sequences create a large repertoire of user instructions and powerful I/O functions which characterize the Model 5.

PROCESSOR FEATURES	
Instruction Set	113 instructions
Instruction Compatibility	INTERDATA Models 3, 4
Instruction Word Lengths	16-bit, 32-bit
Data Word Lengths	8-bit, 16-bit, 32-bit
User Registers	16 accumulators; 15 of these can be used as index registers 8 floating point registers
Memory Addressing	direct addressing up to 64K bytes
Processor I/O	multiplexor bus for up to 256 devices included in processor
Interrupts	Identification of up to 256 levels with automatic vectoring, chaining and queuing. 16 hardware priorities expandable in groups of 16

Memory Modules – The 1-μsec core memory of the Model 5 is expandable in 8K byte modules up to 64K bytes without paging. Addressing can be done at the byte (8-bit) or halfword (16-bit) level.

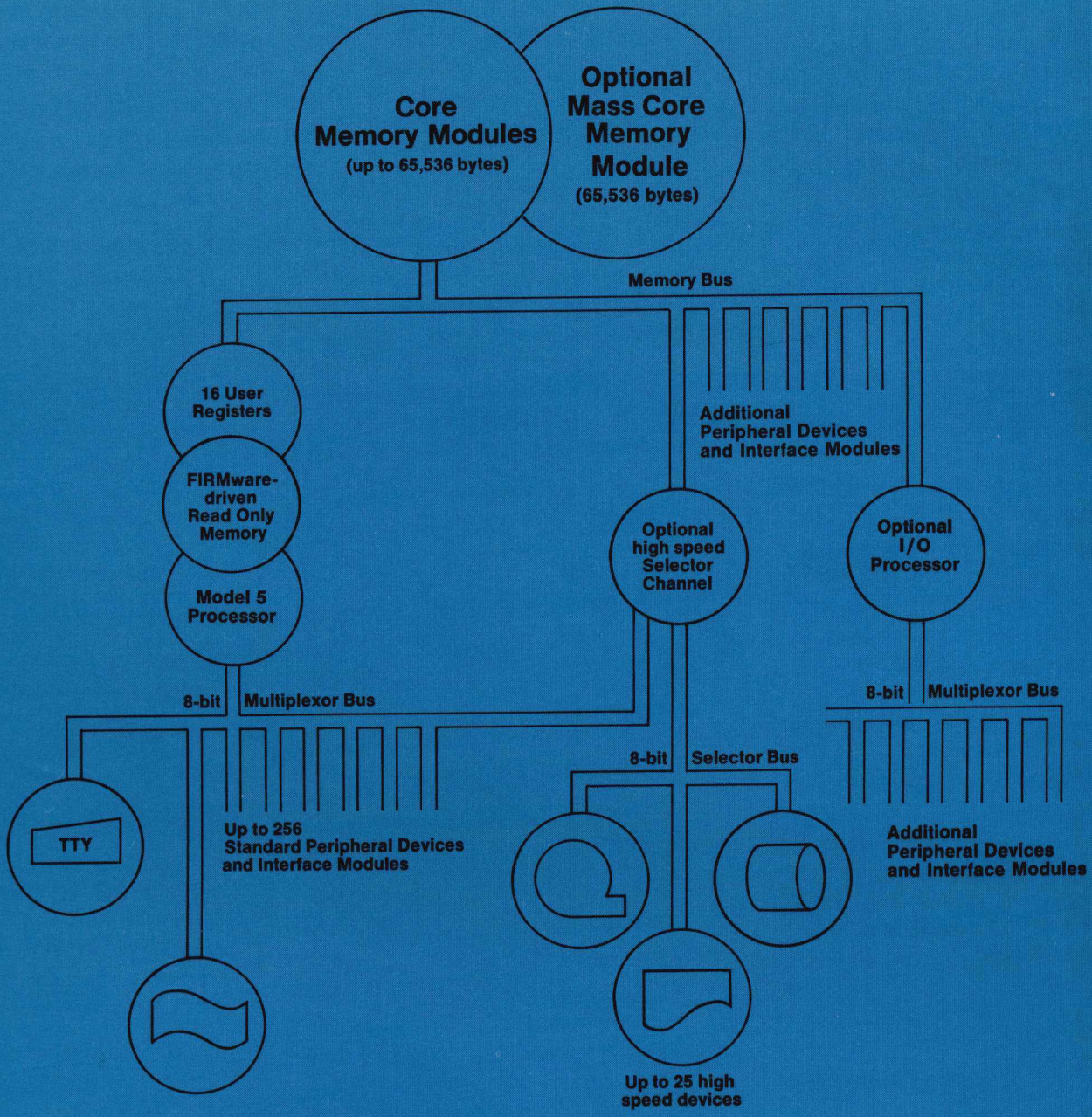
Mass Core Memory – A valuable option of the INTERDATA Model 5 system is a moderate speed, 64K byte Mass Core Memory which is an economical answer for storing large amounts of core-resident software and data. The Mass Core is particularly useful for multi-task real time applications because it minimizes program swapping overhead.

Memory Bus Structure – The Model 5's Memory Bus accommodates up to eight high speed direct memory access devices which are coordinated on a priority managed cycle-stealing basis.

Selector Channel – The Selector Channel is a direct memory access device which provides high speed block-oriented data transfers. Up to 25 devices can be accommodated by the Selector Channel. After the processor initializes the Selector Channel for a block transfer, the processor is free to perform other work.

I/O Processor – This is a powerful facility for expanded systems, particularly where heavy computations are required in combination with extensive input-output. The I/O Processor is a direct memory access element which can take over the bulk of I/O functions in an autonomous manner, relieving the Model 5's main processor for additional tasks. A number of I/O processors can be accommodated by the Model 5's Memory Bus, where each processor can control a large number of I/O devices.

Multi-Level Interrupt Module – This module is provided for applications that require a large number of external interrupts. This multiplexor provides extended interrupt monitoring of additional priority levels, obtainable in groups of 16. A feature of the multiplexor is a built-in real-time clock.



Standard Model 5 Configurations

	MODEL 5/1	MODEL 5/2	MODEL 5/3	MODEL 5/4
Core Memory Modules				
8K Bytes	•			
16K Bytes		•		
32K Bytes			•	•
Memory Protect Module			•	•
High Speed Drum				•
Selector Channel				•
16-line Hardware Interrupt Module			•	•
ASR 33 Teletypewriter	•	•	•	•
High Speed Input/Output Device		•	•	•
Basic Operating System (BOSS)	•	•		
Real Time Operating System (RTOS)			•	•
Fortran IV Compiler		•	•	•
Interactive Fortran	•	•	•	•
Assembler	•	•	•	•

Multi-Task Software

The Model 5's software system is well-integrated with the multi-task approach of its hardware and firmware design. Two advanced operating systems, BOSS and RTOS, form the nucleus of the Model 5's software library.

BOSS –The INTERDATA Basic Operating System is designed to control the smaller configurations. Models 5/1 and 5/2 BOSS provides the user with the operating convenience and support normally found only in much larger systems. It accepts and executes operator-initiated commands, allows overlap of processing and I/O, responds to and services all interrupts, and through the use of logical I/O calls and automatic code conversion provides the user with a high degree of device independence.

BOSS fully supports the operation of the FORTRAN IV compiler and INTERDATA Assembler. Its I/O package contains drivers for all INTERDATA standard peripherals. Its utility package contains the following:

The System Generator is a program designed to allow a user to tailor BOSS to his hardware configuration. It links peripheral drivers into the system, and allows the user to interface special I/O drivers and interrupt routines.

Linking Loader loads object programs from the compiler and assembler and automatically links subroutines. Other features include overlay capability and the preparation of a fast format output suitable for rapid loading.

BOSS Debug is an on-line interactive program that allows examination and modification of core memory. Bias handling is provided for referencing and displaying relocatable programs. Object tapes can be generated for any block of memory, in either 8-bit or standard binary tape formats. Symbolic disassembly of programs from core memory is also provided.

Editor is an on-line interactive text editor allowing direct entry of source statement into memory. These statements can be freely listed, changed, deleted, or augmented while remaining in core memory. Edited statements can then be output to form a source tape.

RTOS is an extremely flexible Real-Time Operating System capable of handling Real-Time Data Acquisition, Process Control and Data Communication applications concurrently with background compilations, assemblies and batch operations. RTOS is available with Model 5/3 and 5/4 configurations.

RTOS fully supports the operation of the FORTRAN IV compiler and INTERDATA Assemblers. Its I/O package contains drivers for INTERDATA standard peripherals and standard system modules. RTOS foreground/background features are:

- Variable foreground/background partitioning
- Variable number of foreground tasks
- Priority and time-oriented scheduling
- Device independence and logical I/O
- Foreground programs can be written in FORTRAN IV.

RTOS permits the scheduling of programs based on real-time events, on elapsed time, and on operator intervention. User programs can request scheduling of other programs in the foreground or in the background. Individual foreground programs can be loaded without disturbing the rest of the system. The background can be employed for any type of user program. At any time, through operator intervention, the background area can be converted to a non-resident foreground area. The RTOS utility packages contain:

System Generator is used for initial system generation. It assembles required I/O modules, allocates core for initial operations and interfaces user-written special purpose routines.

The RTOS Loader is an integral part of the system. It provides full overlay capability for both foreground and background. It can load programs from any suitable device and can output linked load-modules to any output device.

Real-Time Debug provides the same capabilities as BOSS Debug. In addition, it permits debugging of real-time programs by simulating interrupts from real-time devices and handling programs in foreground or background mode.

Editor provides background interactive edit capability as described for BOSS.

Fortran IV allows use of a problem-oriented language for generation of real-time machine language programs. The FORTRAN IV language corresponds to the American Standard Fortran, as defined in USASI Publication X3.9. It is a completely modular, I/O independent program which operates in 16K bytes of memory under BOSS or RTOS.

The FORTRAN IV Compiler generates relocatable object code in one pass. It has been designed to exploit the Model 5's multi-register architecture. The compiler's object code optimization techniques provide for the elimination of redundant expressions and code. The optimization process is enhanced by a complete floating point repertoire. In addition, extensive compile-time diagnostics for program debugging are provided.

Associated with the FORTRAN IV Compiler is a complete Fortran Run-Time Library. The Run-Time Library consists of all basic math and conversion routines as described in ASA Publication #X3.9-1966. The library includes all intrinsic and extrinsic mathematical routines. During execution, the library routines provide error messages for overflow, format errors and other execution-time errors. Additional routines are provided which enable user programs to communicate with the operating system for special functions not defined in the FORTRAN language.

The Model 5 Assembler converts a symbolic source language into a relocatable object form which can be loaded via the Model 5 Operating Systems .The assembler is capable of performing 1, 2 or pass assemblies.

The Model 5 Assembler is available in two versions:

For configuration 5/1, the assembler operates in a stand-alone fashion with the Card Reader or Teletype and High Speed Paper Tape Reader/Punch.

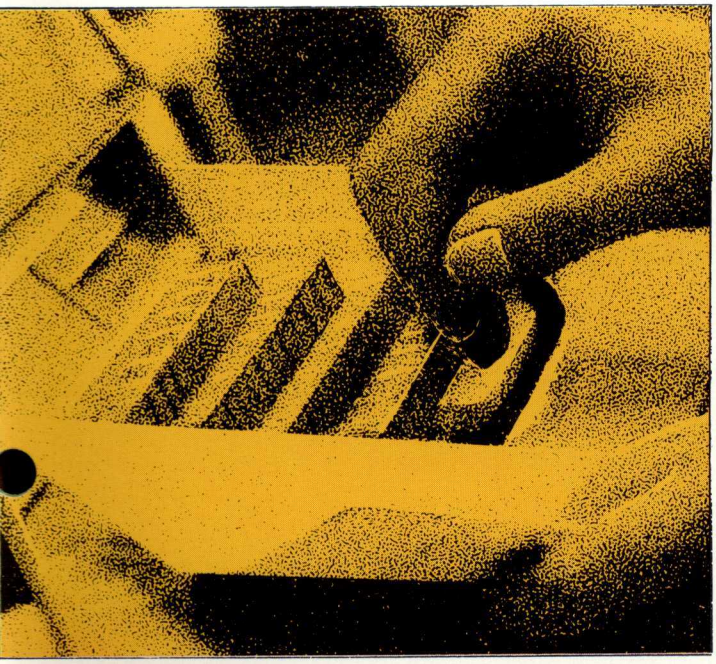
For configurations 5/2 - 5/4, the Model 5 Assembler operates under the BOSS or RTOS, utilizing all devices supported by the Operating System.

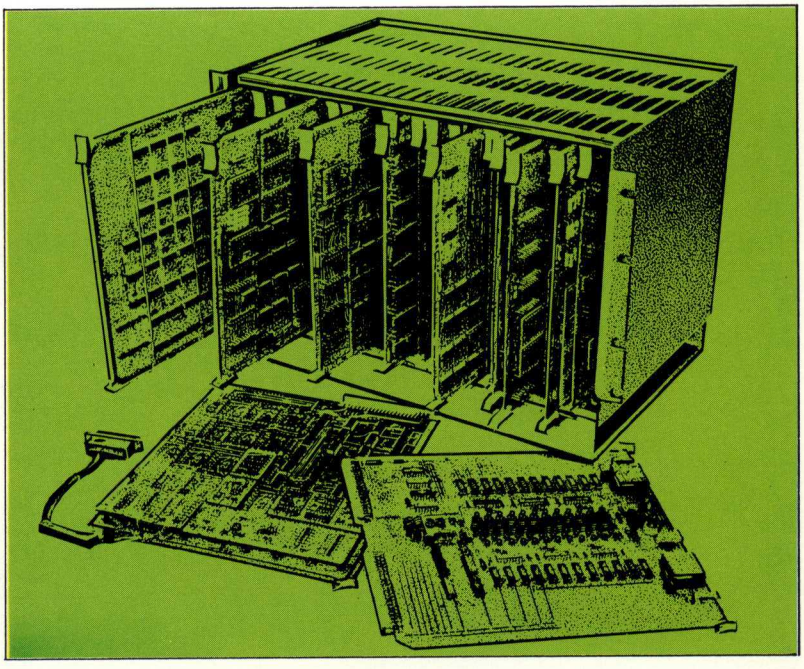
Both assemblers, in addition to translating the normal Model 5 instruction set, have double precision floating-point conversion capability.

Math Library is a complete library of both fixed-point and floating-point arithmetic and conversion routines is available with all configurations of the Model 5.

Task-Oriented Programming Features

The Model 5 is an easy machine to program. Its third generation instruction set (which closely resembles the IBM 360) is complemented by 16 general purpose registers, 8 floating-point registers, direct addressability to 64K bytes and foreground/background facilities. These combine to give the programmer very powerful tools for solving complex real time problems.





The following describes a few of the functions the Model 5 handles with outstanding ease:

Foreground/Background Protection
The Model 5 features **memory protection and privileged instructions** designed to preserve the integrity of the complete system. The memory protect feature, which is available with configurations 5/3 and 5/4, provides area protection. By preventing background programs from destroying foreground routines, it means that compilations, assembles and debugging can safely be performed concurrently with foreground real-time programs. The Model 5's privileged instructions make it possible for an operating system to maintain control of I/O transfers and the loading of Program Status Words.

Foreground/Background Linkage–A Supervisor Call instruction is designed to communicate between user programs and an operating system. This instruction provides a multi-level internal interrupt, which links the sixteen unique entry points to the Operating System. Through this instruction, switching from a protect mode to a supervisor mode is made convenient.

Other supervisory features are provided by Program Status Word instructions which permit loading, saving, or exchanging of supervisor control functions.

For debugging real-time programs, a Simulate Interrupt instruction is provided. This instruction is also useful for triggering real-time interrupt routines under program control.

Processing Operations–The Model 5 features fixed-point multiply and divide instructions. Its complete set of 32-bit floating-point instructions operate on 8 floating-point registers. Both signed and unsigned multiply instructions facilitate either single-precision or multiple-precision computations. Processing operations are made convenient and efficient by a variety of register-to-register instructions, memory reference instructions, and a set of instructions in which one operand is part of the instruction.

Byte handling instructions for load, store, compare and exchange operations, complement the byte-addressability of core memory. An add-to-memory instruction permits every location in memory to be used for counting.

Logical Operations–The Model 5 provides instructions for AND, OR and Exclusive OR operations. These operations can occur between registers, with memory reference, or with immediate operands. Both arithmetic and logical compare instructions apply to 16-bit quantities. The instruction set also contains a valuable instruction for testing individual bits or combinations of bits in a register.

A complete set of conditional branch instructions is provided. The branch instructions can either directly reference any location in memory, or refer to a location relative to the location of the instruction.

The Model 5 can perform variable length shift or rotate operations on either 16 or 32-bit quantities. These shifts can be either logical or arithmetic.

List Processing–General table management is simplified through the use of the Model 5's 15 index registers. In addition, list processing is facilitated by four particular instructions which support push-down stacks and circular lists. The instructions, which are Add to the Top, Remove from the Top, Add to the Bottom, Remove from the Bottom, manipulate lists of variable length up to 510 bytes.

Control Operations –The Branch on Index High and Branch on Index Low or Equal instructions provide fast loop control by combining increment and compare operations into one instruction. The Load Multiple and Store Multiple instructions permit fast loading or storing of a block of from 1 to 16 general registers.

Multi-Task I/O Structure–The task-oriented I/O structure of the Model 5 provides a repertoire of built-in I/O techniques for interrupt management, data transfers and device control. An important benefit is ease of use since an appropriate I/O technique can be chosen and matched to the speed and transfer requirements of various devices. These functions are managed by Operating System software to maintain complete program protection.

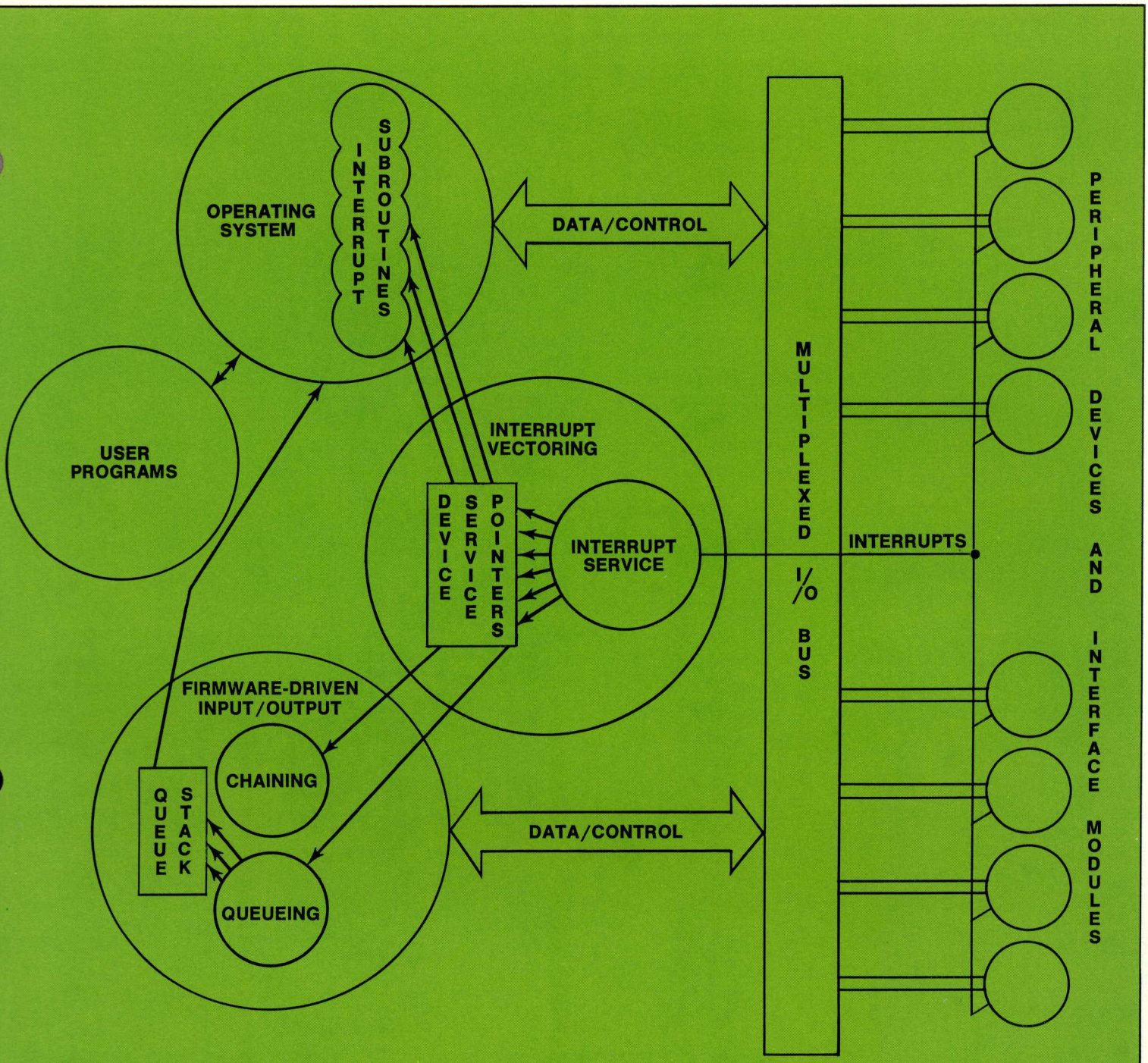
Program-Controlled I/O permits direct communication with I/O devices in either 8-bit or 16-bit transfers.

Interrupt-Driven I/O triggers an appropriate interrupt routine for each device. This efficient interrupt facility relieves the processor from being dedicated to a device while i is transferring data.

Firmware-Driven I/O permits blocks of data to be efficiently transferred to or from devices without interrupting the running program. These facilities can also be used for a variety of pulse counting and external interrupt monitoring functions.

Burst-Mode I/O incorporates Read Block/Write Block instructions. These instructions permit the processor t achieve high transfer rates by momentarily dedicating it to a particular device.

Selector Channel I/O permits devices to transfer data directly to or from the core memory with no processor intervention. Up to 25 devices can be connected to a Selector Channel. Once the Selector Channel is running the processor is no longer involved until the Selector Channel interrupts to indicate termination. Data is transferred to or from memory in 16-bit quantities on a cycle-stealing basis. This method of data transfer is appropriate for any block or record-oriented device which transfers data at a high rate, such as a drum, disc or magnetic tape.



Model 5 I/O Structure

Model 5 I/O Processor This facility is a valuable option for the Model 5. It can relieve the main processor from much of the overhead involved in data transfers, such as starting and stopping devices, data conversion and format control, because the I/O Processor is a dedicated computer.

The I/O Processor is a programmable machine that shares main memory with the Model 5 CPU. Its instruction repertoire is I/O-oriented with particular emphasis on interrupt servicing. As a result, the main processor is free to perform additional functions concurrently.

Interrupt Vectoring is a firmware-driven (microcoded) function which identifies the interrupting device and references a table of pointers. These pointers can direct control to a firmware I/O routine or to a software subroutine unique to the device. Since the swapping of Program Status Words is done automatically by the firmware, and the subroutine is unique to the device, much of the subroutine overhead conventionally needed is eliminated.

Firmware-Driven I/O This microcoded mechanism facilitates data transfer sequences to and from multiple I/O devices without interrupting the program. Upon completion of a transfer, a program interrupt may be generated or chaining/queueing functions can be triggered.

Chaining — This microcoded function permits the linking together of a number of firmware-driven I/O routines without intervention by the software. Both command chaining and data chaining are permitted.

Queueing — This microcoded function permits the automatic entry of information on a circular list (queue stack). Information in the queue stack typically indicates events such as completed transfers and I/O malfunctions. Data in the queue stack can be used for subsequent scheduling of tasks.

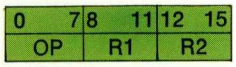
Instruction Repertoire

A simple instruction repertoire may mean months of struggling for your programmers . . . a powerful instruction repertoire will not only make their task much easier, but combined with multiple registers, and other 3rd generation features, will dramatically improve the real-time performance of the system.

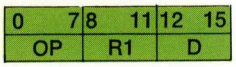
What comprises a powerful instruction repertoire? One manufacturer lists 74 instructions when, in effect, his processor provides only 8 basic functions. Many of the others use the same tactics by listing dozens of trivial combinations.

The Model 5 instruction set has 113 instructions. The basic instruction formats are described below.

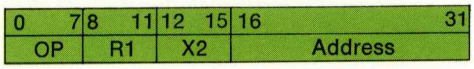
Register to Register format: RR



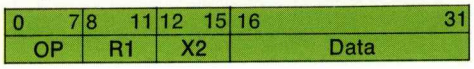
Short Format: SF



Register to Indexed Memory format: RX



Register to Indexed Data format: RS



The system has four instruction formats. The 16-bit halfword instructions are the RR formats. The 32-bit fullword instructions are the RX and RS formats.

The 4-bit R1, R2 (and X2) fields each specify one of the sixteen general registers. Each of the 16 halfword general registers can be used as a fixed-point arithmetic accumulator or as a logical accumulator. Fifteen of the 16 general registers can be used as index registers.

The RR instructions are for operations between the general registers. The R1 and R2 specify the first and second operands respectively. For a register-to-register Add operation [(R1) + (R2) → (R1)].

The SF Short Format instructions include register operations, shifts and branches. With the register operations, the 4-bit data field (D) is used to operate on the general register specified by R1. With the shift instructions, the data field specifies the shift count. With branch instructions, the data field specifies a displacement from the current location counter.

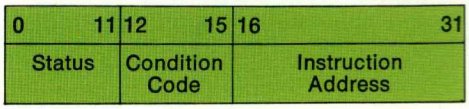
The RX instructions are for operations between the general registers and memory. The R1 field specifies the first operand and the sum of the index register (X2) and Address fields specify the address of the second operand. For a register-to-indexed memory Add operation [(R1) + (Address + (X2)) → (R1)].

Immediate instructions (RS) are included for shifting and branching. Operations involving immediate operands also use the RX format. For the immediate instruction the R1 field specifies the first operand and the sum of the contents of the index register (X2) and Address field form the second operand. For an Add immediate operation, [(R1) + Address + (X2) → (R1)]. The shift count is given by [Address + (X2)].

Instruction Alignment — Halfword RR and SF format instructions and fullword RX and RS format instructions are aligned on halfword boundaries. This permits mixing of halfword and fullword instructions with no requirement for halfword NO-OP's to force correct fullword instruction memory alignment.

Program Status Word — Defines the status of the machine, the instruction address and a condition code. Status bits consist of interrupt masks and control bits. The condition code reflects the carry, overflow, greater than and less than zero flags for various operations.

Program Status Word



Instruction Repertoire

Type	Instruction	Mnemonic
Load and Store Instructions	Load Halfword (RR)	LHR
	Load Halfword	LH
	Load Halfword Immediate	LHI
	Load Immediate Short	LIS
	Load Complement Short	LCS
	Load Multiple	LM
	Store Halfword	STH
	Store Multiple	STM
Fixed Point Arithmetic Instructions	Add Halfword (RR)	AHR
	Add Halfword	AH
	Add Halfword Immediate	AHI
	Add Immediate Short	AIS
	Add Halfword to Memory	AHM
	Add with Carry Halfword (RR)	ACHR
	Add with Carry Halfword	ACH
	Subtract Halfword (RR)	SHR
	Subtract Halfword	SH
	Subtract Halfword Immediate	SHI
	Subtract Immediate Short	SIS
	Subtract with Carry Halfword (RR)	SCHR
	Subtract with Carry Halfword	SCH
	Compare Halfword (RR)	CHR
	Compare Halfword	CH
	Compare Halfword Immediate	CHI
	Multiply Halfword (RR)	MHR
	Multiply Halfword	MH
	Multiply Halfword Unsigned (RR)	MHUR
	Multiply Halfword Unsigned	MHU
	Divide Halfword (RR)	DHR
	Divide Halfword	DH
Floating Point Instructions	Add (RR)	AER
	Add	AE
	Subtract (RR)	SER
	Subtract	SE
	Compare (RR)	CER
	Compare	CE
	Multiply (RR)	MER
	Multiply	ME
	Divide (RR)	DER
	Divide	DE
	Load (RR)	LER
	Load	LE
	Store	STE
Fixed Point Logical Instructions	AND Halfword (RR)	NHR
	AND Halfword	NH
	AND Halfword Immediate	NHI
	OR Halfword (RR)	OHR
	OR Halfword	OH
	OR Halfword Immediate	OHI
	Exclusive OR Halfword (RR)	XHR
	Exclusive OR Halfword	XH
	Exclusive OR Halfword Immediate	XHI
	Compare Logical Halfword (RR)	CLHR
	Compare Logical Halfword	CLH
	Compare Logical Halfword Immediate	CLHI
	Test Halfword Immediate	THI
Shift Instructions	Shift Right Halfword Logical	SRHL
	Shift Right Short Logical	SRSL
	Shift Right Logical (fullword)	SRL
	Shift Left Halfword Logical	SLHL
	Shift Left Short Logical	SLSL
	Shift Left Logical (fullword)	SLL
	Shift Right Halfword Arithmetic	SRHA

Type	Instruction	Mnemonic
	Shift Right Arithmetic (fullword)	SRA
	Shift Left Halfword Arithmetic	SLHA
	Shift Left Arithmetic (fullword)	SLA
	Rotate Right Logical (fullword)	RRL
	Rotate Left Logical (fullword)	RLL
Byte Handling Instructions	Load Byte (RR)	LBR
	Load Byte	LB
	Store Byte (RR)	STBR
	Store Byte	STB
	Exchange Byte (RR)	EXBR
	Compare Logical Byte	CLB
Branch Instructions	Branch on True Condition (RR)	BTCR
	Branch on True Condition	BTC
	Branch on True Condition Forward	BTFS
	Branch on True Condition Backward	BTBS
	Branch on False Condition (RR)	BFCR
	Branch on False Condition	BFC
	Branch on False Condition Forward	BFFS
	Branch on False Condition Backward	BFBS
	Branch AND Link (RR)	BALR
	Branch AND Link	BAL
	Branch on Index High	BXH
	Branch on Index Low or Equal	BXLE
Extended Mnemonics Instructions	Branch on Zero	BZ
	Branch on Not Zero	BNZ
	Branch on Plus	BP
	Branch on Not Plus	BNP
	Branch on Minus	BM
	Branch on Not Minus	BNM
	Branch on Carry	BC
	Branch on Overflow	BO
	Branch on Low	BL
	Branch on Not Low	BNL
	Branch on Equal	BE
	Branch on Not Equal	BNE
	No Operation (RR)	NOPR
	No Operation	NOP
Status Control Instructions	Load Program Status Word	LPSW
	Exchange Program Status (RR)	EPSR
	Supervisor Call	SVC
List Handling Instructions	Add to Top of List	ATL
	Add to Bottom of List	ABL
	Remove from Top of List	RTL
	Remove from Bottom of List	RBL
Input-Output Instructions	Autoload	AL
	Simulate Interrupt	SINT
	Read Data (byte) (RR)	RDR
	Read Data (byte)	RD
	Read Halfword (RR)	RHR
	Read Halfword	RH
	Read Block (RR)	RBR
	Read Block	RB
	Write Data (byte) (RR)	WDR
	Write Data (byte)	WD
	Write Halfword (RR)	WHR
	Write Halfword	WH
	Write Block (RR)	WBR
	Write Block	WB
	Sense Status (RR)	SSR
	Sense Status	SS
	Output Command (RR)	OCR
	Output Command	OC
	Acknowledge Interrupt (RR)	AIR
	Acknowledge Interrupt	AI

A Full Complement of System Modules

These modules provide the user with a group of general interfaces to reduce or eliminate design effort. As an example, modules are provided to handle 8-bit or 16-bit parallel input or output, manual data entry and decimal indicators in 4 or 8 decades.

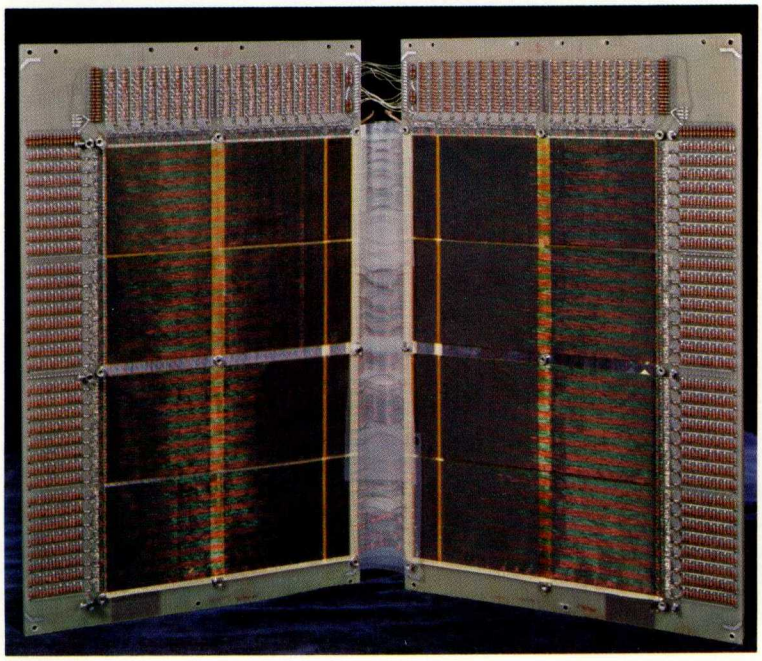
Modules for Digital Data Input The Sense Line Module provides the user with 16 lines, which may be used for detecting the status of devices on command from the Model 5. The Sense Switch Module enables the operator to enter program variables manually through 16 switches. The Manual Data Entry modules make available 8 or 16 decades of thumbwheel switches and a "data entry" push button to the operator.

Modules for Digital Data Output The Control Line Module provides 16 buffered control lines for the activation of external events. The Relay Closure Module provides 16 isolated relay closures with storage registers for the operation of medium power external devices. The Decimal Indicator Modules provide 4 or 8 decades of decimal indicators with or without a decimal point.

Modules for Digital Input-Output The Byte and Halfword Input-Output modules make available 8 (or 16) stored data input lines, 8 (or 16) stored data output lines, 8 control lines, 8 sense lines and one priority interrupt line to the user. The Digital Multiplexor provides a very economical set of modular building blocks to monitor or control up to 2048 lines with a single controller using input or output modules of 128 lines. These modules can be intermixed in any fashion. The Digital Multiplexor utilizes a biased core technique to insure absolute DC isolation from the sense contact and an excellent common mode transient response and DC offset capability. These features make the unit particularly suitable for use in noisy environments.

Modules for a Total Design Effort The General Purpose Interface Module provides the engineer with buffering to the Input-Output Multiplexor Bus, address logic and interrupt logic to facilitate customized interface design. The Standard Memory Bus Interface provides the user with buffering to the High Speed Memory Bus to aid in the design of specialized Direct Memory Access Channels.

Modules for Analog Input-Output The Analog to Digital Conversion equipment provides fully interfaced conversion from bipolar analog signals in the ± 10 volt range with resolutions of 8, 10 and 12 bits, with or without a sample and hold amplifier. This system can multiplex



up to 64 analog channels in both random or sequential modes. Just like the Analog to Digital equipment, the Digital to Analog Multiplexor provides fully interfaced conversion to bipolar analog signals in the ± 10 volt range with resolutions of 8, 10 and 12 bits. This system can multiplex up to 16 channels in random or sequential modes. Each channel uses dual rank registers with an operational amplifier.

Proven Peripherals

A broad range of field proven peripherals are available to the Model 5 user, to meet the requirements of various applications.

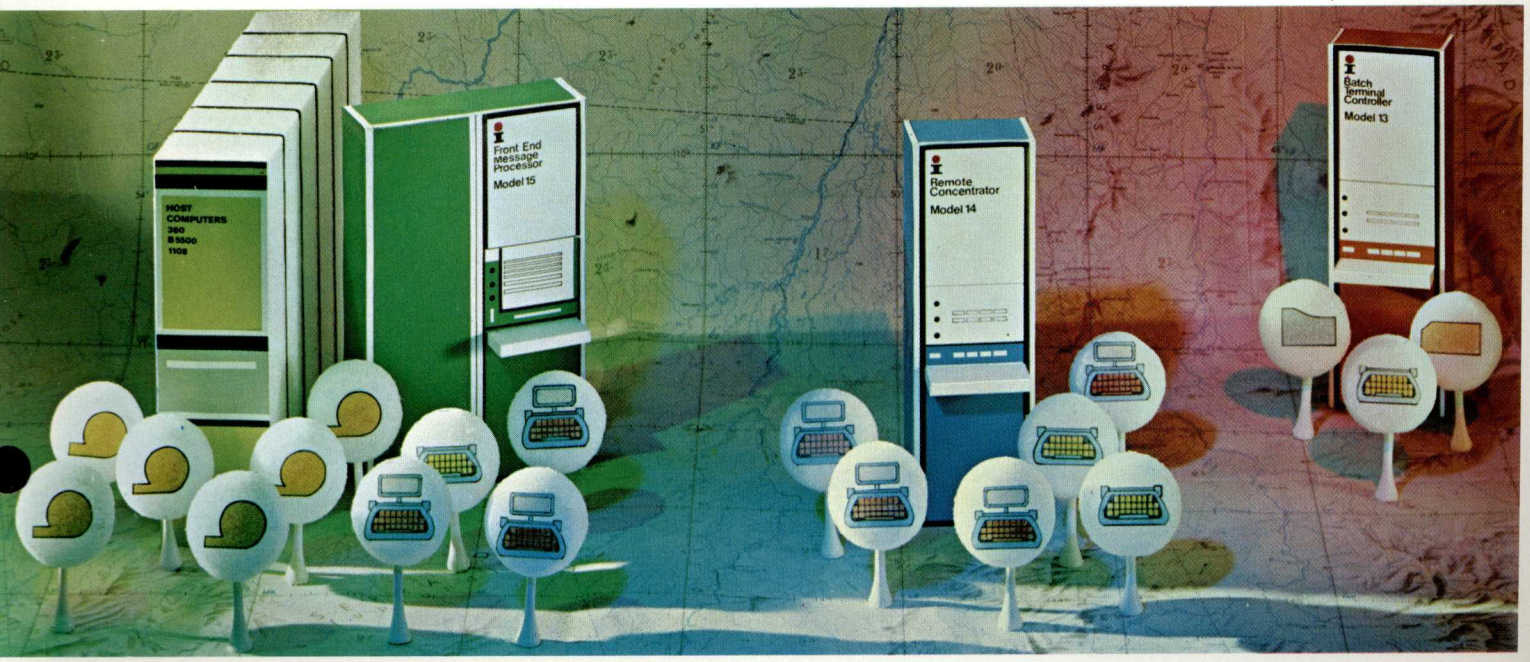
Drums and Magnetic Tapes Fast access bulk storage media is offered in 131KB to 8.3MB sizes. Average transfer rates are 230K bytes per second with 8.7 and 17.4 millisecond average access times. IBM compatible seven and nine track tape transports are available for the Model 5 with 25 ips speed and densities of 556 and 800 bpi. The Mini Disc System is a rugged, reliable and inexpensive mass storage system with 51.2K bytes of storage per disc. Up to two discs can be operated on each controller. Average access time is 8.5 milliseconds and the transfer rate is 60K bytes per second. The unit operates over a wide temperature range.

Paper Tape Input-Output A 300 cps Reader and 60 cps Punch are offered for the Model 5, individually, or as a complete package. Fan-fold tape is featured as the software media.

The Line Printer provides 300 lpm capability with 132 columns per line and 64 characters. Ideally suited to fulfill your high speed listing requirements.

The Card Reader is a 200 cpm reader, provided for card oriented input systems.

The Cassette Tape System provides a reliable and inexpensive substitute for paper tape input-output equipment. The transfer rate is 300 characters per second, with up to 250K bytes of storage for each cassette.



Complete Data Communications Hardware

Character oriented modules are available to allow the connection of remote terminals or processors over telephone lines to the Model 5 system.

Data Set Adapter These modules enable the Model 5 to communicate with Bell type 103, 202, 201 and 301 data sets. The adapters are double buffered and optionally generate and check character parity. The Bell 801 Automatic Dialer adapter enables the Model 5 system to establish a connection over switched telephone lines automatically.

Host Computer Interfaces The INTERDATA/IBM 360 interface provides a direct hardware connection to the Multiplexor or Selector Channel of the IBM 360 processor. Parity is generated and checked on each character transferred. The INTERDATA/Burroughs 5500 Interface is a pseudo-magnetic tape unit and it is connected to the Burroughs 5500 through a B5000 Tape Control Unit. Six bit characters are transferred to/from the B5000. Horizontal and longitudinal parity is checked and generated in the interface. Binary or alphanumeric character format is selectable under program control. The INTERDATA/Univac 1108 Interface operates on a Normal or Compatible Channel in the ESI mode. Parity is checked and generated in the interface.

Customer Support

With hundreds of installed computer systems, INTERDATA maintains an extensive program of customer support activities. You are encouraged to avail yourself of these services in order to effectively utilize the Model 5's capabilities.

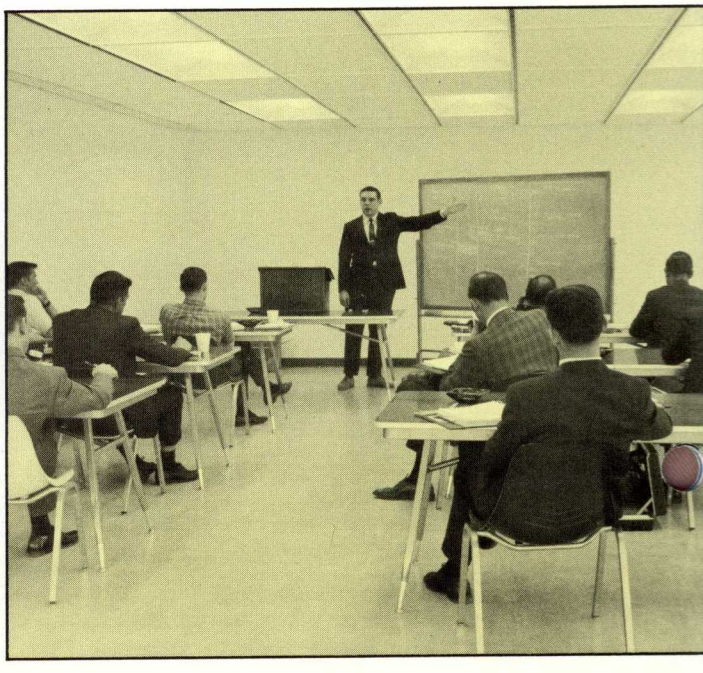
Customer Training — Hundreds of customers attend the INTERDATA year-round training school. Additional training is provided on-site where requested. Courses pertinent to the Model 5 include: software and hardware instruction, firmware instruction and a special course in maintenance.

Field Service — Qualified factory trained personnel are at your disposal **24 hours a day** should you experience difficulty with your Model 5, and they are as close as your nearest INTERDATA sales office.

Application Support — For the many customers who require special support, INTERDATA offers a senior team of hardware, software, and firmware specialists whose background includes data acquisition systems, testing systems, process control systems and data communications. INTERDATA sales engineers have long experience with small compu applications. They can give you valuable local assistance in planning and dimensioning your application.

Interchange — The INTERDATA user's group is an active and growing association. By sharing software and special interfaces, customers gain a valuable "second level" of support.

Quality Control — Quality Control at INTERDATA begins with detailed mechanical and electrical inspection of all components utilized in manufacturing a Model 5. Each stage of assembly is carefully monitored through the employment of automatic and semi-automatic test equipment. Logic boards, for example, are checked with our own computers. In addition, ALL computers are given extensive environmental chamber evaluation prior to shipment. This total approach to Quality Control insures quick, trouble-free installation and a high degree of reliabilit



Model 5
Specifications

Data Word Length — 8, 16, 32 bits (parity optional)

Memory Cycle Time —
1.0 microsecond — Core Memory
[illegible]00 nanosecond — Read-only-memory

[illegible]ord Size — 16 bits

General Registers — 16 hardware registers (16 bits each)

Floating-Point Registers — 8 total, each is 32 bits long

Index Registers — 15 hardware general registers may be used for indexing

Basic Memory — 8K bytes, expandable to 64K bytes

Directly Addressable Memory — 64K bytes

Arithmetic — Two's Complement

Instruction Repertoire — 113 standard instructions including floating point arithmetic and privileged instructions

16 bit — Load Halfword — 2.8 microseconds
16 bit — Add Halfword — 3.2 microseconds
16 bit — Multiply — 28 microseconds

Typical Micro-Instruction, Execution Time — 400 nsec.
16 bit — Micro Add — 0.800 microseconds
16 bit — Micro Load — 0.400 microseconds

Input/Output

Program Transfer — 30K bytes/sec

Block Transfer — 150K bytes/sec
500K bytes/sec (with selector)

Firmware I/O — 30K bytes/sec

Priority Interrupts — Identification of up to 256 levels with automatic vectoring chaining and queuing.

16 Hardware priorities expandable in groups of 16

Display Panel

Control Switches — Power, initialize, execute
Mode Control — Run, halt, single op, variable speed, address input, memory read, memory write

Speed Control — Variable, 1 cycle/sec to 100 cycles/sec

Display — Two registers simultaneously selectable

Switches — Sixteen data/address/sense

Mechanical

Size — 66 inch RETMA standard cabinet, dimensions 66″ x 22½″ x 30″

Power — 600 watts, 115 VAC ± 10%, single phase, 47-63 hertz

Weight — 175 lbs.

Temperature:
Operating — 0° to 50° C
Storage — 55° to 85° C

Humidity — 0 to 90% relative

Reliability

Processor — MTBF - 7321 Hrs.
8K bytes Memory MTBF - 10,915 Hrs.

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